



DIAMOND SYSTEMS CORPORATION

ONYX-MM-XT

PC/104 Format
Counter/Timer & Digital I/O Module
User Manual V1.4



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1. General Information and Features

ONYX-MM is a PC/104-compliant I/O module with 48 digital I/O lines, 3 16-bit counter/timers, and 3 interrupts. It is an 8-bit module, so it does not contain the 16-bit expansion bus connector. This connector is available as an option by requesting the –B16 suffix when ordering.

Three right-angle pin headers are provided for I/O. Two identical 50-pin (2x25) headers contain 24 digital I/O lines each and +5/ground, and a third 14-pin (2x7) header provides the counter/timer signals, external interrupt pin, and +5/ground. J2, with 24 digital I/O lines, is on the right side of the module in the standard PC/104 I/O position. J3, with 24 additional digital I/O lines, is on the left side of the module, and J4, with the counter/timer and interrupt signals, is on the top edge of the module. (The bottom edge of the module is defined as the edge with the PC/104 ISA bus connectors.)

All I/O signals are TTL compatible.

The boards operate on +5V power supply only.

Digital I/O

48 TTL digital I/O lines are provided by 2 82C55 chips (24 per chip). Each line can source 2.5mA in a logic 0 state and sink 2.5mA in a logic 1 state. I/O lines are unbuffered, i.e. there is a direct connection between the 82C55 and the I/O header. Bit C0 of each 82C55 can be used to generate an interrupt on the PC bus (see **Interrupts** below).

All digital I/O lines are connected to +5V through 10K Ω pull-up resistors.

Digital I/O lines are accessed through two 50-pin headers, J3 and J4, with 24 lines (one 82C55) on each header. See page 8 for I/O header pinouts.

Counter/Timer I/O

Onyx-MM contains three 16-bit counter/timers provided by an 82C54 chip. Each counter/timer has an input pin, a gate pin, and an output pin. The input pin responds to positive edges. The gate pin is active high; a counter will count whenever its associated gate pin is high and will not count when the gate pin is low. The input and gate pins are connected to +5V through 10K Ω pull-up resistors.

Counter/timer I/O lines are accessed through a 14-pin header J5. See page 8 for the pinout of J5.

An on-board oscillator provides a 4MHz clock that can be used to drive any counter. Each counter has a maximum input rate of 10MHz.

Programmable features include input source selection and counter cascading:

Counter 0 input can be either IN0 from the I/O header or 4MHz.

Counter 1 input can be either IN1, 4MHz, or Counter 0 output.

Counter 2 input can be either IN2, 4MHz, or Counter 1 output.

All three counter outputs can be programmed to generate PC bus interrupts as described below. With appropriate configuration, two or three counters can be cascaded to form a 32-bit or 48-bit counter, and the output of this cascaded counter can generate an interrupt.

Interrupts

ONYX-MM provides a means to generate up to three active-high interrupt signals on the PC/104 bus. Three pin headers are provided to select interrupt levels for each interrupt signal. Interrupt levels 2 through 7 are available on each header.

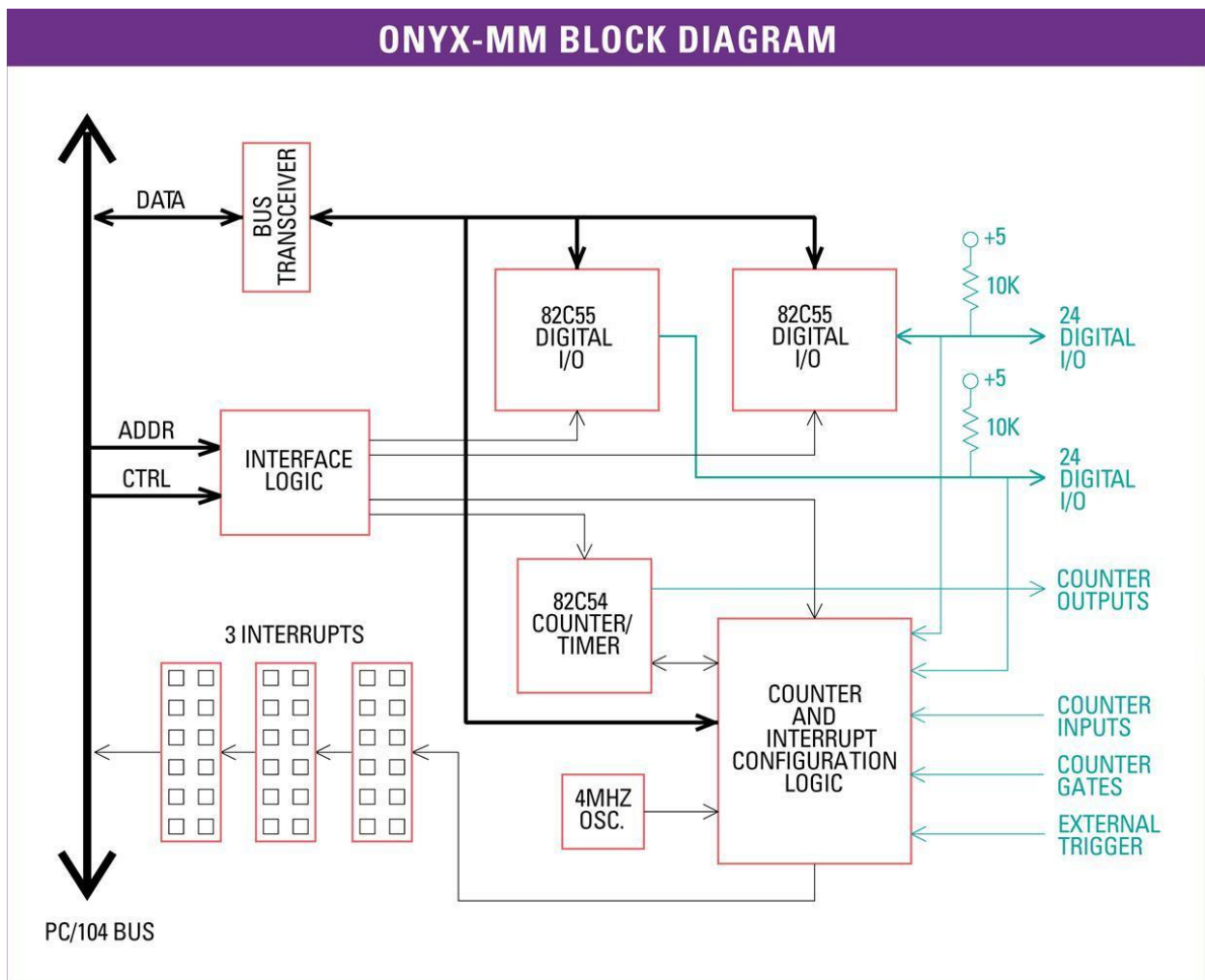
To enable interrupt sharing, a 1K Ω pull-down resistor can be jumpered to each interrupt line, and interrupt signals are driven by tristate drivers. When an interrupt is pending, the interrupt line is driven high, and when it is not pending, the output is in high-impedance mode, and the 1K Ω resistor pulls it down to a logic 0 state.

Interrupt sources are programmable. Interrupts can be generated from both digital I/O and counter/timer signals as follows:

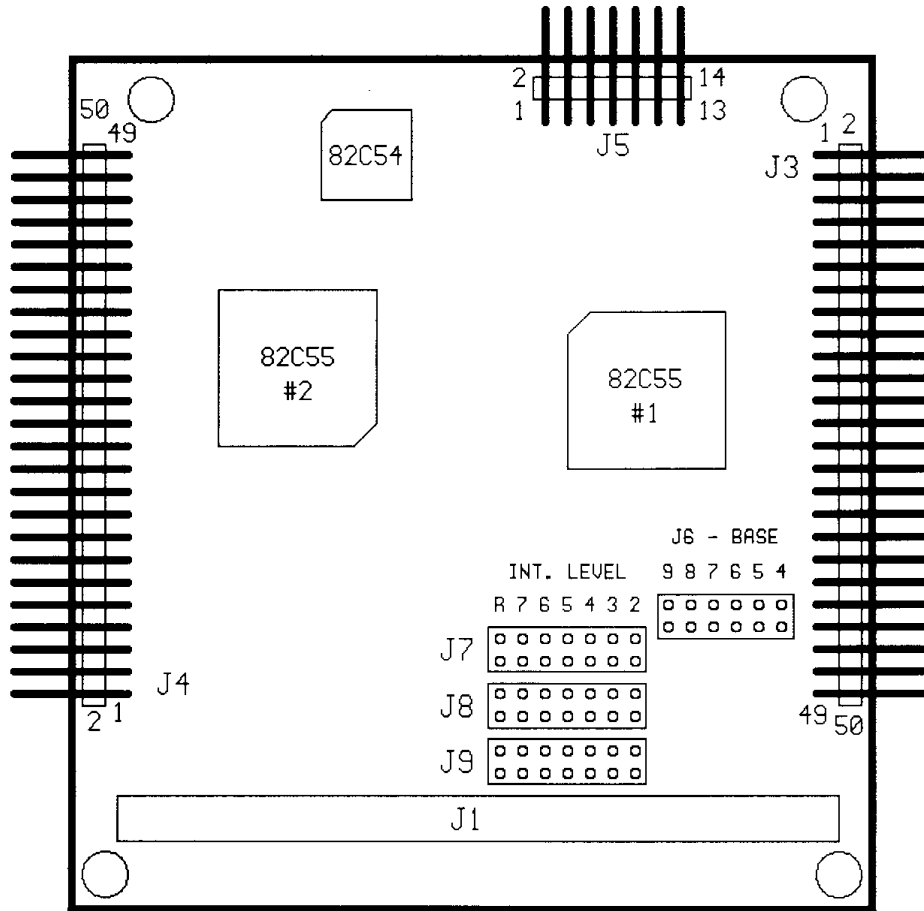
- Interrupt no. 1: Bit C0 from 82C55 #1 or Counter 0 output
- Interrupt no. 2: Bit C0 from 82C55 #2 or Counter 1 output
- Interrupt no. 3: External interrupt pin or Counter 2 output

Interrupts are enabled and disabled under software control by manipulating a control register.

Block Diagram



2. Board Drawing



Item	Description
J1	PC/104 bus connector
J3	Digital I/O ports 1A, 1B, 1C
J4	Digital I/O ports 2A, 2B, 2C
J5	Counter/timer signals
J6	Board base address configuration
J7	Interrupt 0 configuration
J8	Interrupt 1 configuration
J9	Interrupt 2 configuration

3. I/O Header Pinouts

J3: Digital I/O Header for 82C55 #1

J4: Digital I/O Header for 82C55 #2

Each of these headers is identical in pinout. They provide 24 digital I/O lines, +5, and ground. Pin 1 of J3 is in the upper right corner of the board, and pin 1 of J4 is in the lower left corner.

A7	1	2	Gnd
A6	3	4	Gnd
A5	5	6	Gnd
A4	7	8	Gnd
A3	9	10	Gnd
A2	11	12	Gnd
A1	13	14	Gnd
A0	15	16	Gnd
C7	17	18	Gnd
C6	19	20	Gnd
C5	21	22	Gnd
C4	23	24	Gnd
C3	25	26	Gnd
C2	27	28	Gnd
C1	29	30	Gnd
C0	31	32	Gnd
B7	33	34	Gnd
B6	35	36	Gnd
B5	37	38	Gnd
B4	39	40	Gnd
B3	41	42	Gnd
B2	43	44	Gnd
B1	45	46	Gnd
B0	47	48	Gnd
+5	49	50	Gnd

J5: Counter/Timer and Interrupt Header

This header is a 14-pin header with all counter/timer signals, the external interrupt pin, +5, and ground.

In 0	1	2	In 1
Gate 0	3	4	Gate 1
Out 0	5	6	Out 1
In 2	7	8	External Interrupt
Gate 2	9	10	Gnd
Out 2	11	12	Gnd
+5	13	14	Gnd

4. Base Address Configuration

ONYX-MM's base address is set with header J6, located at the lower right corner of the board. Each of the six pairs of pins on J6 corresponds to a different address bit. A pair left open is equal to a 1, and a pair with a jumper installed is equal to a 0. The header is used to select address bits 9-4, resulting in an 16-byte I/O decode. The leftmost pair selects address bit A9, and the rightmost pair selects address bit A4. Although any 16-byte location is selectable, certain locations are reserved or may cause conflicts. The table below lists recommended base address settings for ONYX-MM. The default setting is 300 Hex. "Open" means an open position, and "Inst" means a position with a jumper installed.

Base Address		Header J6 Position					
Hex	Decimal	9	8	7	6	5	4
220	544	Open	Inst	Inst	Inst	Open	Inst
240	576	Open	Inst	Inst	Open	Inst	Inst
250	592	Open	Inst	Inst	Open	Inst	Open
260	608	Open	Inst	Inst	Open	Open	Inst
280	640	Open	Inst	Open	Inst	Inst	Inst
290	656	Open	Inst	Open	Inst	Inst	Open
2A0	672	Open	Inst	Open	Inst	Open	Inst
2B0	688	Open	Inst	Open	Inst	Open	Open
2C0	704	Open	Inst	Open	Open	Inst	Inst
2D0	720	Open	Inst	Open	Open	Inst	Open
2E0	736	Open	Inst	Open	Open	Open	Inst
300	768 (Default)	Open	Open	Inst	Inst	Inst	Inst
330	816	Open	Open	Inst	Inst	Open	Open
340	832	Open	Open	Inst	Open	Inst	Inst
350	848	Open	Open	Inst	Open	Inst	Open
360	864	Open	Open	Inst	Open	Open	Inst
380	896	Open	Open	Open	Inst	Inst	Inst
390	912	Open	Open	Open	Inst	Inst	Open
3A0	928	Open	Open	Open	Inst	Open	Inst
3C0	960	Open	Open	Open	Open	Inst	Inst
3E0	992	Open	Open	Open	Open	Open	Inst

5. Interrupt Configuration

Each interrupt signal has its own configuration jumper block. The jumper block configures the interrupt level and the 1K Ohm pull-down resistor. A pull-down resistor is required on each active interrupt line on the PC/104 bus. Only one resistor should be installed per interrupt level for the entire system.

J7: Interrupt #0

J8: Interrupt #1

J9: Interrupt #2

Position	Function	Open	Jumper
R	1K Ohm Resistor	No pulldown	Pulldown (max 1 per level)
7	IRQ7		
6	IRQ6		
5	IRQ5		
4	IRQ4		
3	IRQ3		
2	IRQ2		

Install only one jumper in each header in any of these 6 locations to select the interrupt level

All three interrupt sources can be set to the same level if desired. However only one pulldown resistor should be installed for each interrupt level.

6. Register Map

Base +	Function	Comments
0	DIO port 1A	0 - 3 are 82C55 #1 registers
1	DIO port 1B	
2	DIO port 1C	
3	DIO port 1 configuration register	4 - 7 are 82C55 #2 registers
4	DIO port 2A	
5	DIO port 2B	
6	DIO port 2C	
7	DIO port 2 configuration register	8 - 11 are 82C54 registers
8	Counter/timer 0 data	
9	Counter/timer 1 data	
10	Counter/timer 2 data	
11	Counter/timer mode configuration register	
12	Counter/timer input configuration register	
13	(maps to register 12)	
14	Interrupt configuration register	
15	(maps to register 14)	

Note that locations 12 and 13 both map to the same physical register on Onyx-MM. Likewise locations 14 and 15 both map to the same physical register on the board.

7. Register definitions

Base + 0: Digital I/O Register A, 82C55 no. 1

Bit	7	6	5	4	3	2	1	0
Name	1A7	1A6	1A5	1A4	1A3	1A2	1A1	1A0

1A7-1A0 Digital I/O port 1A, port A on 82C55 no. 1

Base + 1: Digital I/O Register B, 82C55 no. 1

Bit	7	6	5	4	3	2	1	0
Name	1B7	1B6	1B5	1B4	1B3	1B2	1B1	1B0

1B7-1B0 Digital I/O port 1B, port B on 82C55 no. 1

Base + 2: Digital I/O Register C, 82C55 no. 1

Bit	7	6	5	4	3	2	1	0
Name	1C7	1C6	1C5	1C4	1C3	1C2	1C1	1C0

1C7-1C0 Digital I/O port 1C, port C on 82C55 no. 1

Base + 4: Digital I/O Register A, 82C55 no. 2

Bit	7	6	5	4	3	2	1	0
Name	2A7	2A6	2A5	2A4	2A3	2A2	2A1	2A0

2A7-2A0 Digital I/O port 2A, port A on 82C55 no. 2

Base + 5: Digital I/O Register B, 82C55 no. 2

Bit	7	6	5	4	3	2	1	0
Name	2B7	2B6	2B5	2B4	2B3	2B2	2B1	2B0

2B7-2B0 Digital I/O port 2B, port B on 82C55 no. 2

Base + 6: Digital I/O Register C, 82C55 no. 2

Bit	7	6	5	4	3	2	1	0
Name	2C7	2C6	2C5	2C4	2C3	2C2	2C1	2C0

2C7-2C0 Digital I/O port 2C, port C on 82C55 no. 2

Base + 3: Digital I/O Configuration Register, 82C55 no. 1

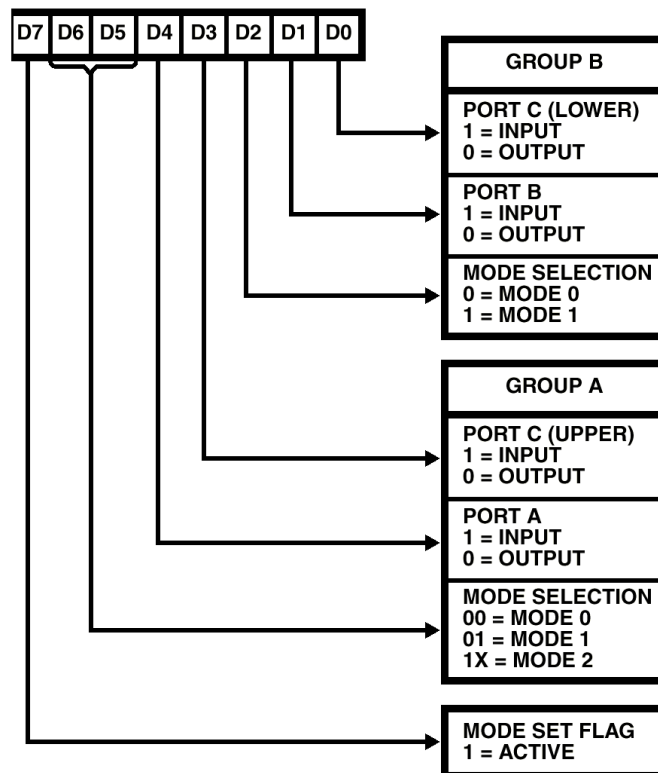
Base + 7: Digital I/O Configuration Register, 82C55 no. 2

These control registers determine the direction and mode of the 82C55 digital I/O lines. The diagram below comes from the 82C55 chip datasheet which is included at the back of this manual. Base + 3 is the control register for chip 1, and Base + 7 is the control register for chip 2.

Most applications use the simple I/O configuration in which bit 7 is set to 1 and the Mode is set to 0 for all ports.

Here is a list of common configuration register control bytes:

Configuration Byte		Port A	Port B	Port C (both halves)
Hex	Decimal			
9B	155	Input	Input	Input
92	146	Input	Input	Output
99	153	Input	Output	Input
90	144	Input	Output	Output
8B	139	Output	Input	Input
82	130	Output	Input	Output
89	137	Output	Output	Input
80	128	Output	Output	Output



Base + 8: Counter/Timer 0 Data

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

D7-D0 Divisor bits 7-0 or 15-8

Base + 9: Counter/Timer 1 Data

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

D7-D0 Divisor bits 7-0 or 15-8

Base + 10: Counter/Timer 2 Data

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

D7-D0 Divisor bits 7-0 or 15-8

Base + 11: Counter/Timer Configuration

The diagram below is from the 82C54 datasheet which is included at the back of this manual.

D₇	D₆	D₅	D₄	D₃	D₂	D₁	D₀
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC — Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

M — MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW — Read/Write:

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

The registers described below are built in to the Onyx-MM circuitry and are separate from the 82C55 and 82C54 chips. In the register maps below, blank locations are unused. See the accompanying schematic diagrams on the following pages.

Base + 12: Counter/timer input configuration register

Bit	7	6	5	4	3	2	1	0
Name				S21	S20	S11	S10	S0

S21 - S20 Counter 2 input select:

S21	S20	Input source
0	0	In2
0	1	4MHz oscillator
1	X	Out1

S11 - S10 Counter 1 input select:

S11	S10	Input source
0	0	In1
0	1	4MHz oscillator
1	X	Out0

S0 Counter 0 input select

0	In0
1	4MHz oscillator

Base + 14: Interrupt configuration register

Bit	7	6	5	4	3	2	1	0
Name			SRC2	SRC1	SRC0	INTE2	INTE1	INTE0

SRC2 Interrupt source 2:

0	External interrupt pin
1	Counter 2 output

SRC1 Interrupt source 1:

0	Bit C0 from 82C55 #2 (base + 6, bit 0)
1	Counter 1 output

SRC0 Interrupt source 0:

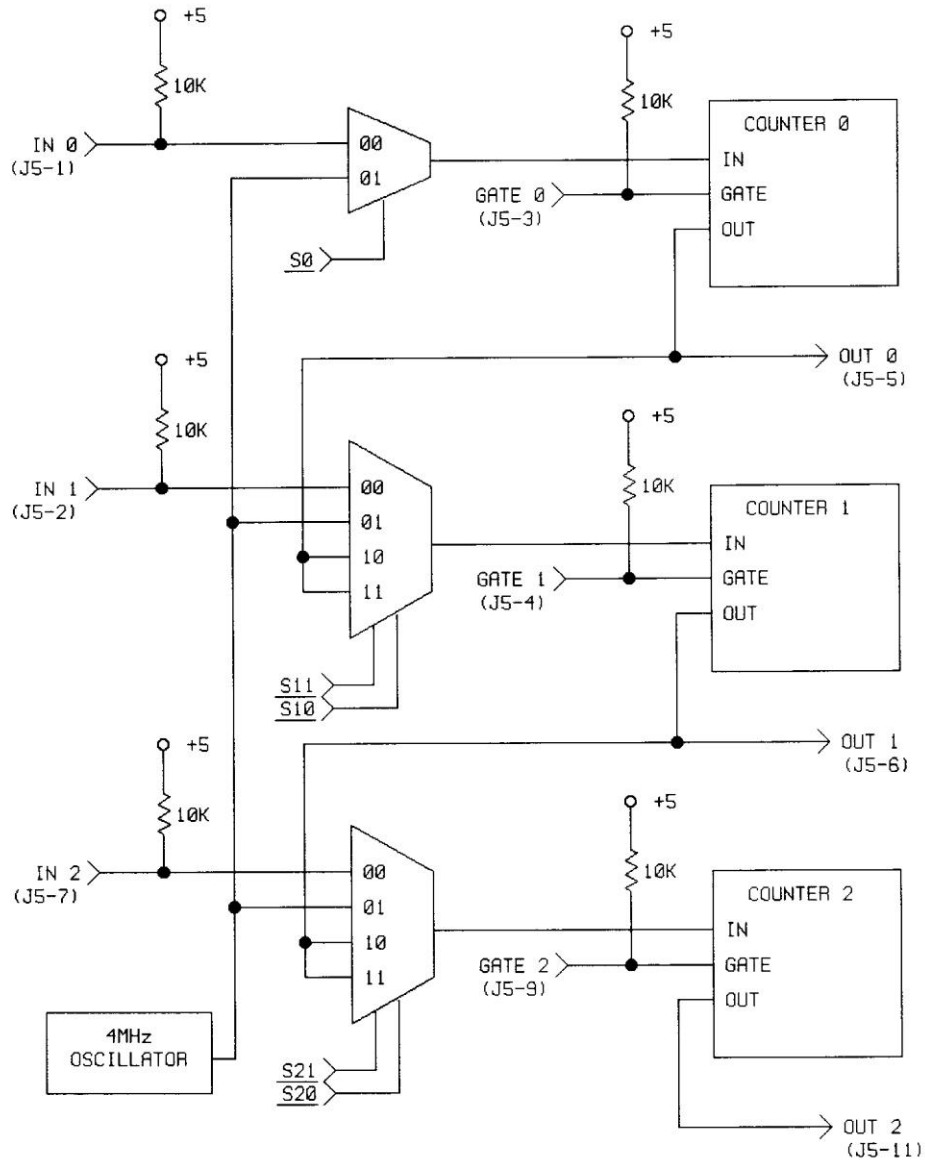
0	Bit C0 from 82C55 #1 (base + 2, bit 0)
1	Counter 0 output

INTE2 - 0 Interrupt enable signals

0	Disabled
1	Enabled

8. Counter/Timer Circuit Schematic

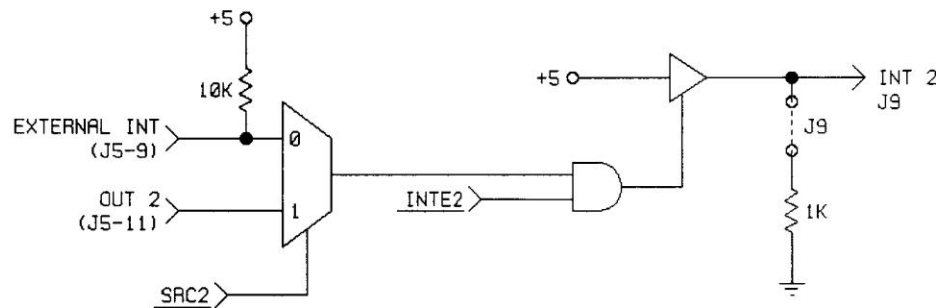
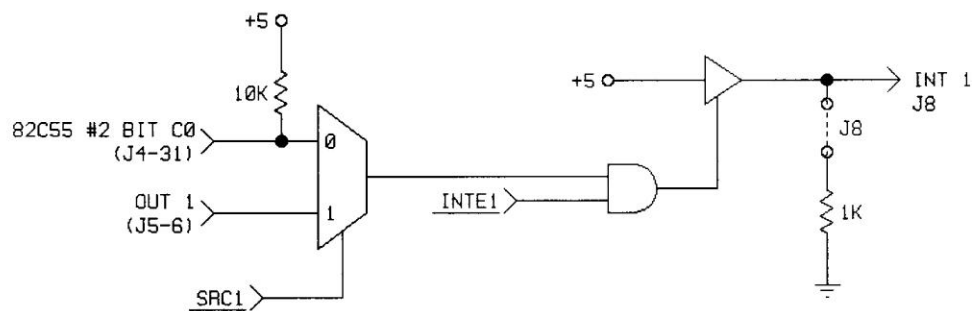
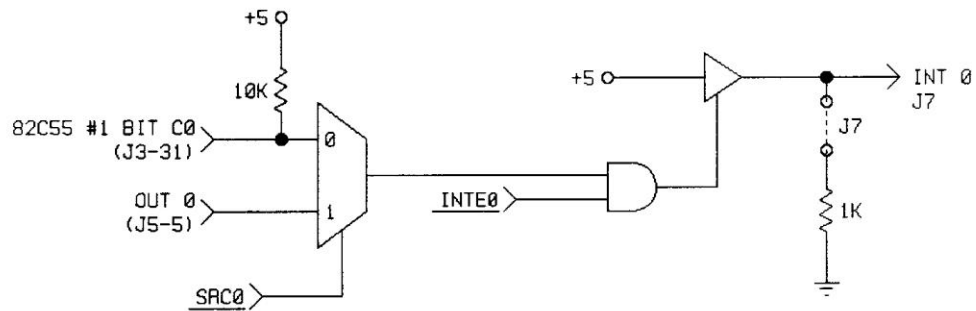
The schematic below illustrates the counter/timer configuration and how the counter/timer input configuration register controls it. See the control register description on page 13.



S20 UNDERLINE INDICATES CONTROL REGISTER BIT
(J5-11) PARENTHESES INDICATE I/O HEADER AND PIN NO.

9. Interrupt Circuit Schematic

The schematic below illustrates the interrupt circuit configuration and how the interrupt configuration register controls it. See the control register description on page 13.



INTE2 UNDERLINE INDICATES CONTROL REGISTER BIT
 (J5-11) PARENTHESES INDICATE I/O HEADER AND PIN NO.

10. Specifications

Counter/Timer Circuitry

Chip	82C54-2
Counter/timers	3, 16 bits wide
Maximum input frequency	10MHz
On-board oscillator	4MHz \pm .01% (100 ppm)
Signal type	TTL
Input voltage, all inputs:	
Low	-0.5V min, 0.8V max
High	2.0V min, 5.5V max
Input current	-200 μ A max (low), 2 μ A max (high)
Output voltage, all outputs:	
Low	0.0V min, 0.4V max
High	3.0V min, V _{cc} - 0.4V max
Output current	\pm 2.5mA max, each line
Pullup resistors	10K Ω all input lines

Digital I/O Circuitry

Chip	82C55A (x2)
Number of I/O lines	48
Direction	All lines programmable for input or output in groups of 4/8
Input voltage:	
Low	-0.5V min, 0.8V max
High	2.0V min, 5.5V max
Output voltage:	
Low	0.0V min, 0.4V max
High	3.0V min, V _{cc} - 0.4V max
Output current	\pm 2.5mA max, each line
Pullup resistors	10K Ω all lines

Interrupt Circuitry

No. of interrupts	3
Pull-down resistor	1K Ω resistor selectable via jumper on each interrupt
Interrupt levels	2 - 7

General

Dimensions	3.550" x 3.775"
Power supply (V _{cc})	5.0VDC \pm 10%, 200mA typical (all outputs open)
Card type	8-bit PC/104 bus compliant
Temperature range	-40 - +85°C, operating and storage